**module** full\_add(a,b,cin,sum,cout);

**inpu**t a,b,cin;

**output** sum,cout;

**wire** x,y,z;

// instantiate building blocks of full adder

**half\_add** h1(.a(a),.b(b),.s(x),.c(y));

**half\_add** h2(.a(x),.b(cin),.s(sum),.c(z));

**or** o1(cout,y,z);

**endmodule** : full\_add

// code your half adder design

**module** half\_add(a,b,s,c);

**input** a,b;

**output** s,c;

// gate level design of half adder

**xor** x1(s,a,b);

**and** a1(c,a,b);

**endmodule** :half\_add